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(54) **INSTRUCTION CONVERTING APPARATUS USING PARALLEL EXECUTION CODE**

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(57) **ABSTRACT**

A processor can decode short instructions with a word length equal to one unit field and long instructions with a word length equal to two unit fields. An opcode of each kind of instruction is arranged into the first unit field assigned to the instruction. The number of instructions to be executed by the processor in parallel is s. When the ratio of short to long instructions is s-1:1, the s-1 short instructions are assigned to the first unit field to the $s\text{-}1^{th}$ unit field in the parallel execution code, and the long instruction is assigned to the s^{th} unit field to the $(s+k-1)^{th}$ unit field in the same parallel execution code.

33 Claims, 29 Drawing Sheets